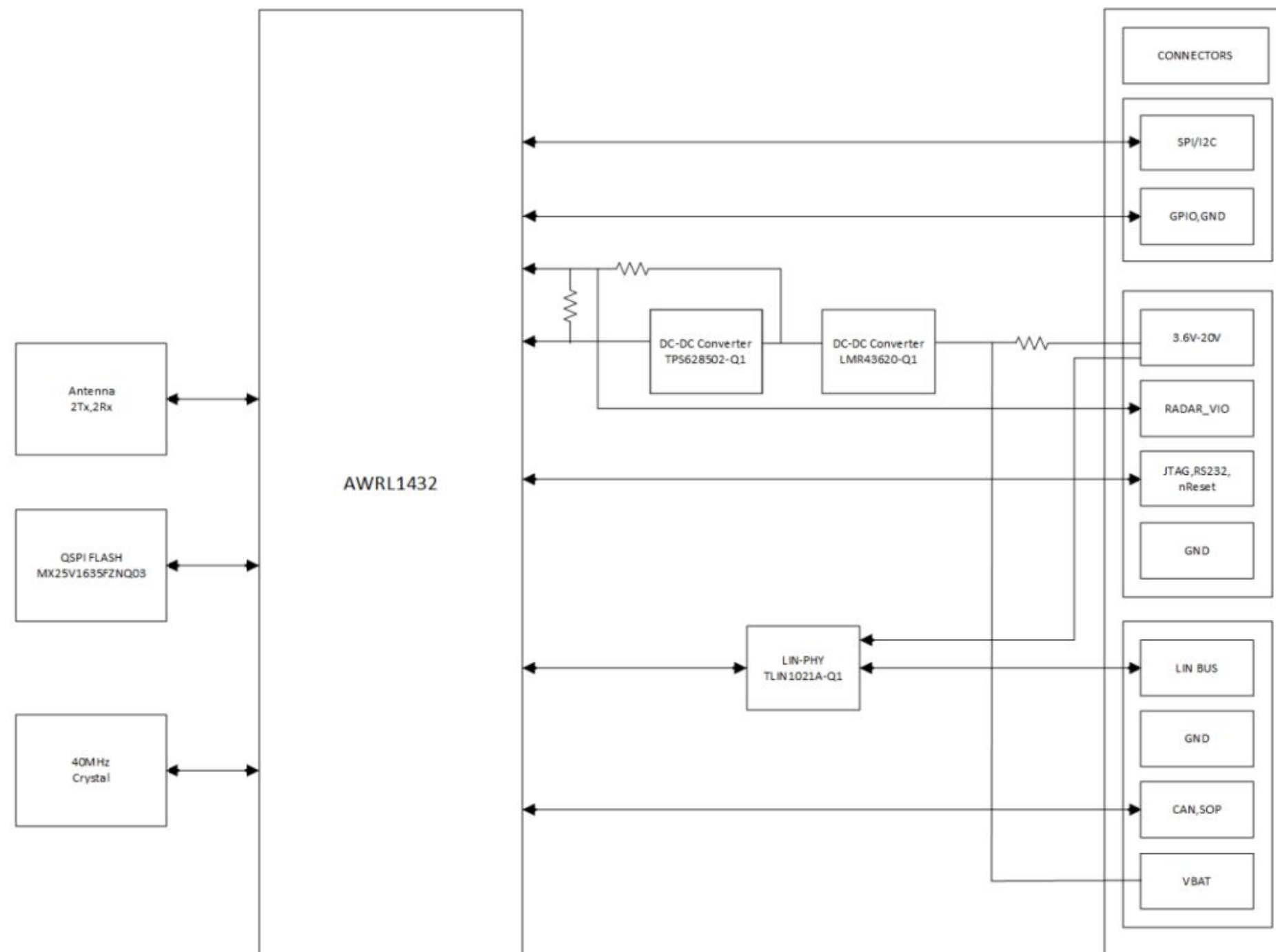



## Revision History

Rev	ECN #	Approved Date	Approved by	Notes

## BLOCK DIAGRAM



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Orderable: <a href="#">N / A</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 9/24/2024	 <b>TEXAS INSTRUMENTS</b>
TID #: <a href="#">TIDEP-01036</a>	Project Title: <a href="#">AWRL 1432 KTO Reference Design</a>		
Number: <a href="#">TIDEP-01036</a>   Rev: <a href="#">A</a>	Sheet Title: <a href="#">BLOCK DIAGRAM</a>		
SVN Rev: Not in version control	Assembly Variant: <a href="#">001_AWR</a>	Sheet: <a href="#">1</a> of <a href="#">7</a>	
Drawn By: <a href="#">Texas Instruments</a>	File: <a href="#">AWRL1432KTO_Block_Diagram.SchDoc</a>	Size: B	
Engineer: <a href="#">Texas Instruments</a>	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	<a href="http://www.ti.com">http://www.ti.com</a>	© Texas Instruments 2022

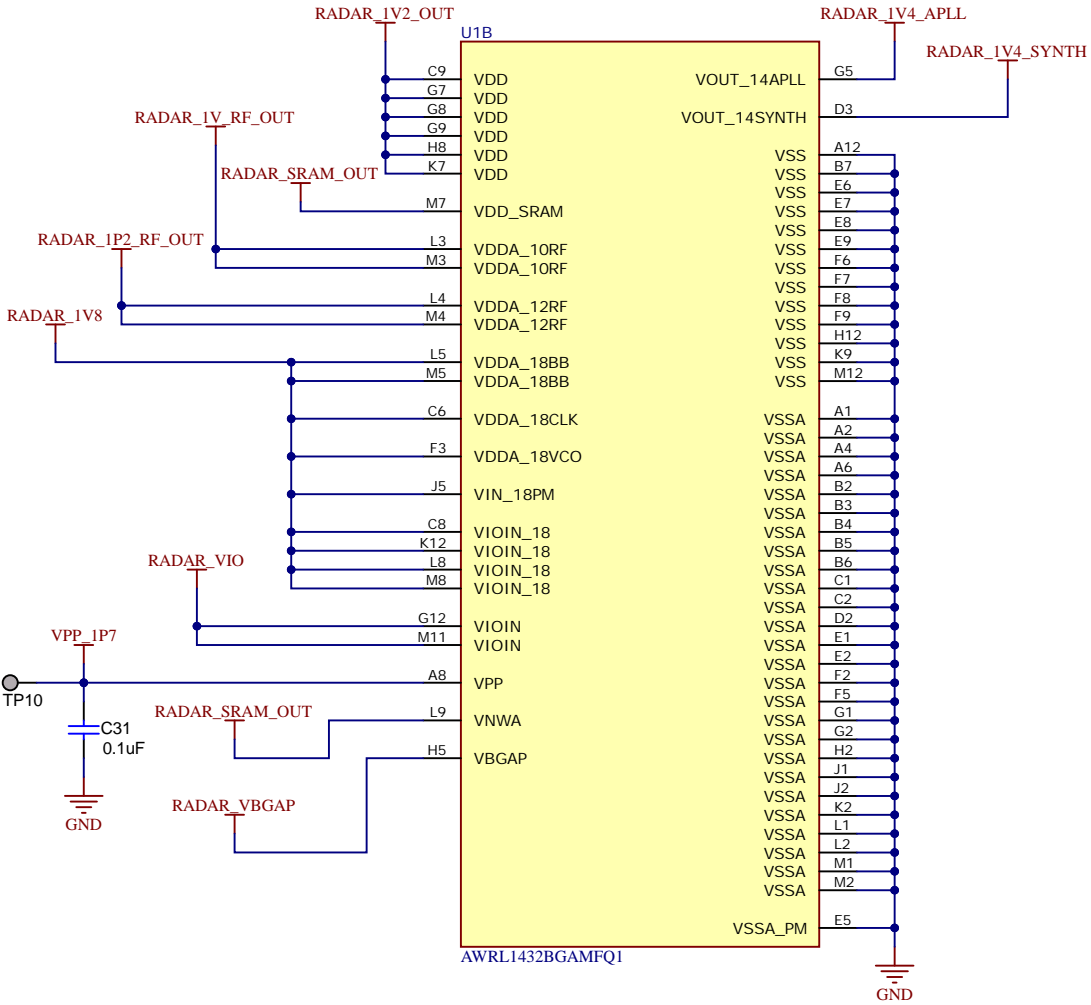
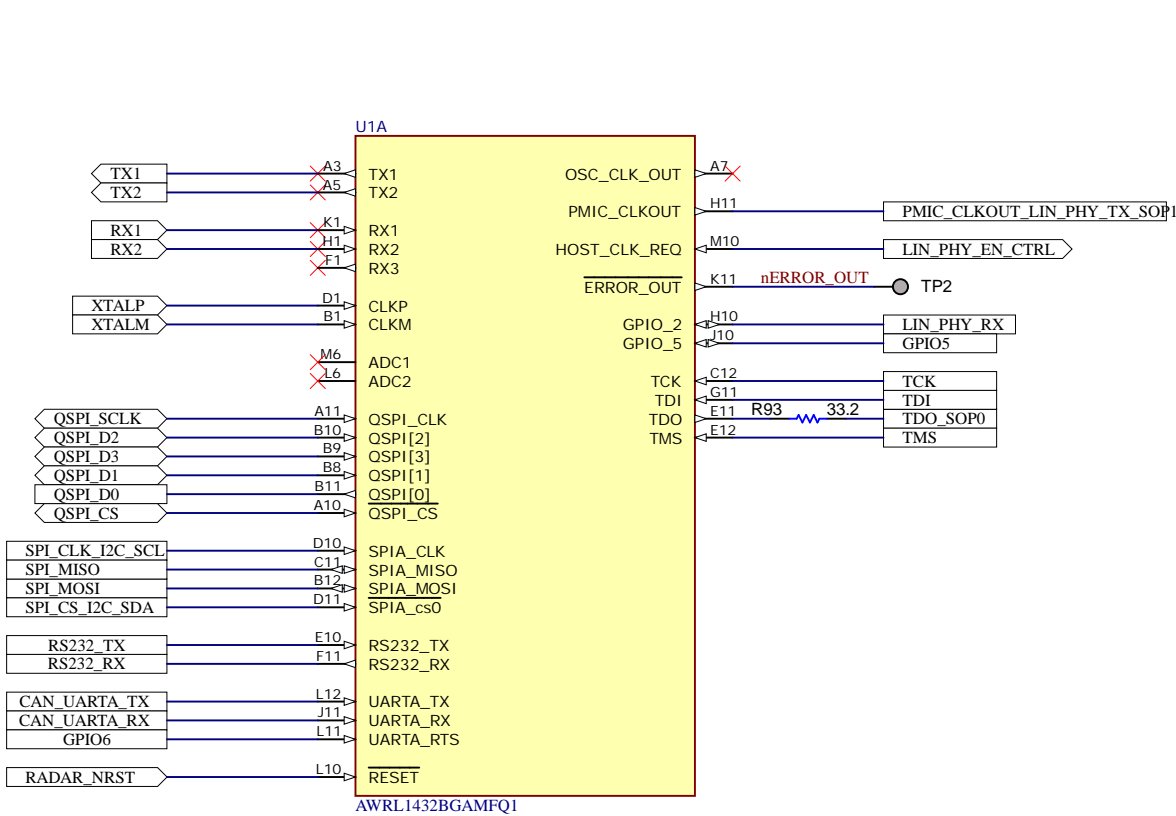
1	2	3	4	5	6
A					A
B					B
C					C
D					D

TABLE OF CONTENTS

SHEET NO.	SHEET NAME
1	BLOCK DIAGRAM
2	TABLE OF CONTENTS
3	xWRL1432_CHIP
4	DECOUPLING_CAPS_QSPI
5	BUCK_REGULATORS_SOP_CTRL
6	LIN_PHY_CONNECTORS
7	EVM_HARDWARE

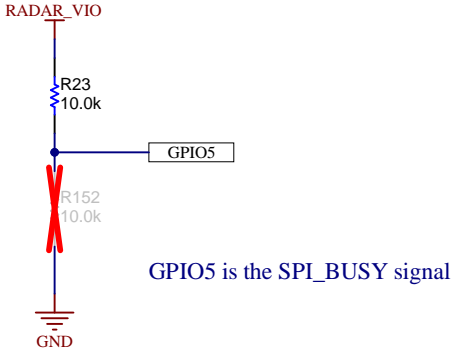
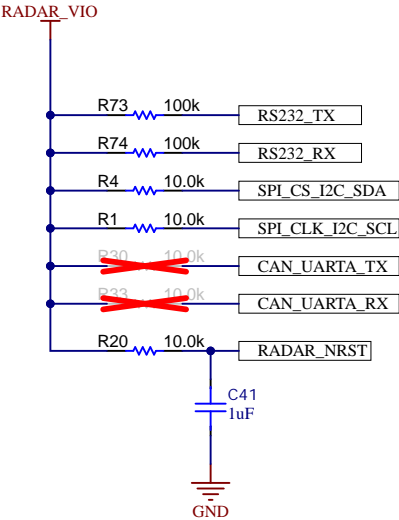
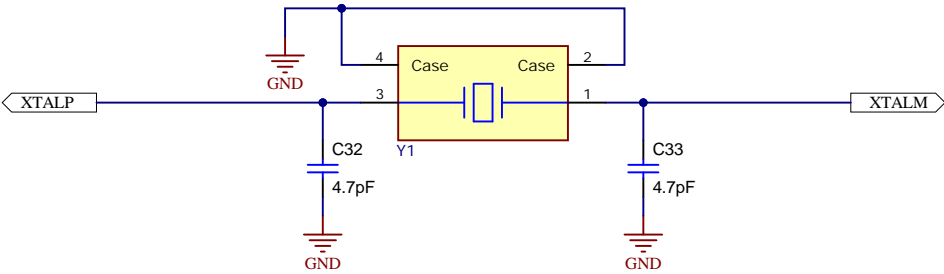
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xWRL1432 CHIP



**Design Note:**  
1. Antenna traces are GCPW traces  
2. 'Generic No ERCs' were placed intentionally on Single Port RF Tx, Rx lines

40 MHz CRYSTAL OSCILLATOR



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A

A

B

B

C

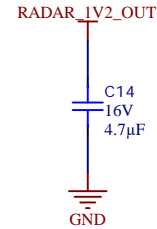
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D

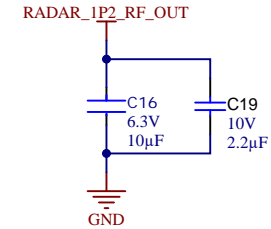
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# SUPPLY\_DECOUPLING\_CAPS

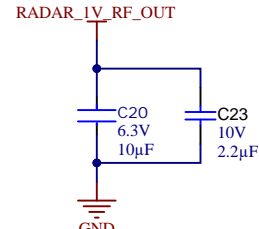
1V2\_OUT DIG SUPPLY



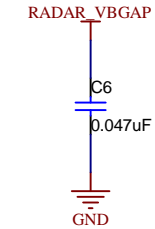
1V2\_RF\_OUT SUPPLY



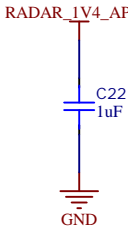
1V\_RF\_OUT SUPPLY



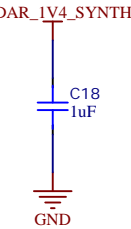
VBGAP SUPPLY



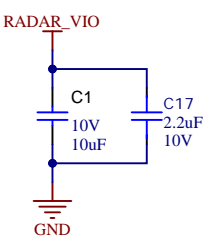
VOUT\_PLL SUPPLY



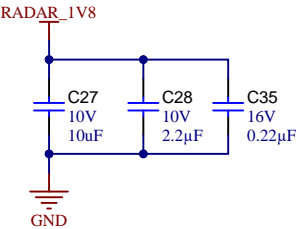
VOUT\_SYNTH SUPPLY



RADAR 3V3 VIO SUPPLY

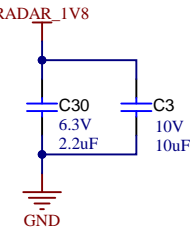


RADAR 1V8 SUPPLY

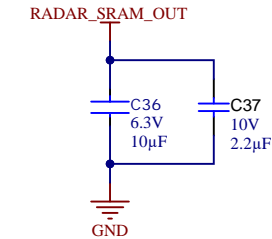


Common 10µF+2.2µF+0.22µF for PM, VCO\_LDO, BB, VCLK supply

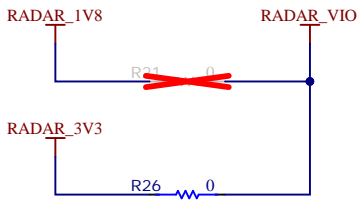
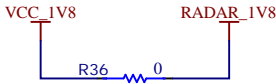
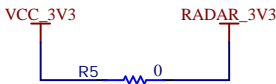
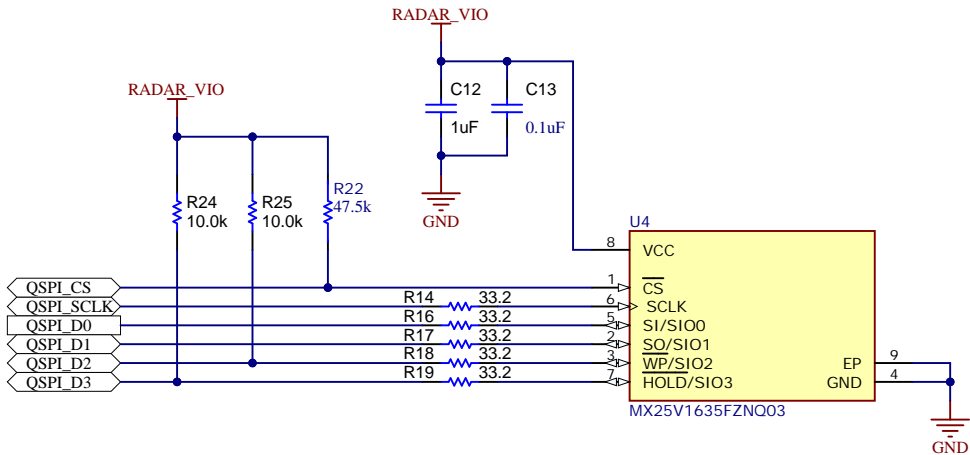
1V8\_IO SUPPLY



SRAM\_OUT SUPPLY



# QSPI FLASH



## Design Note:

Default VIO is 3.3V, Mount R21 and DNP R26 for 1.8V VIO



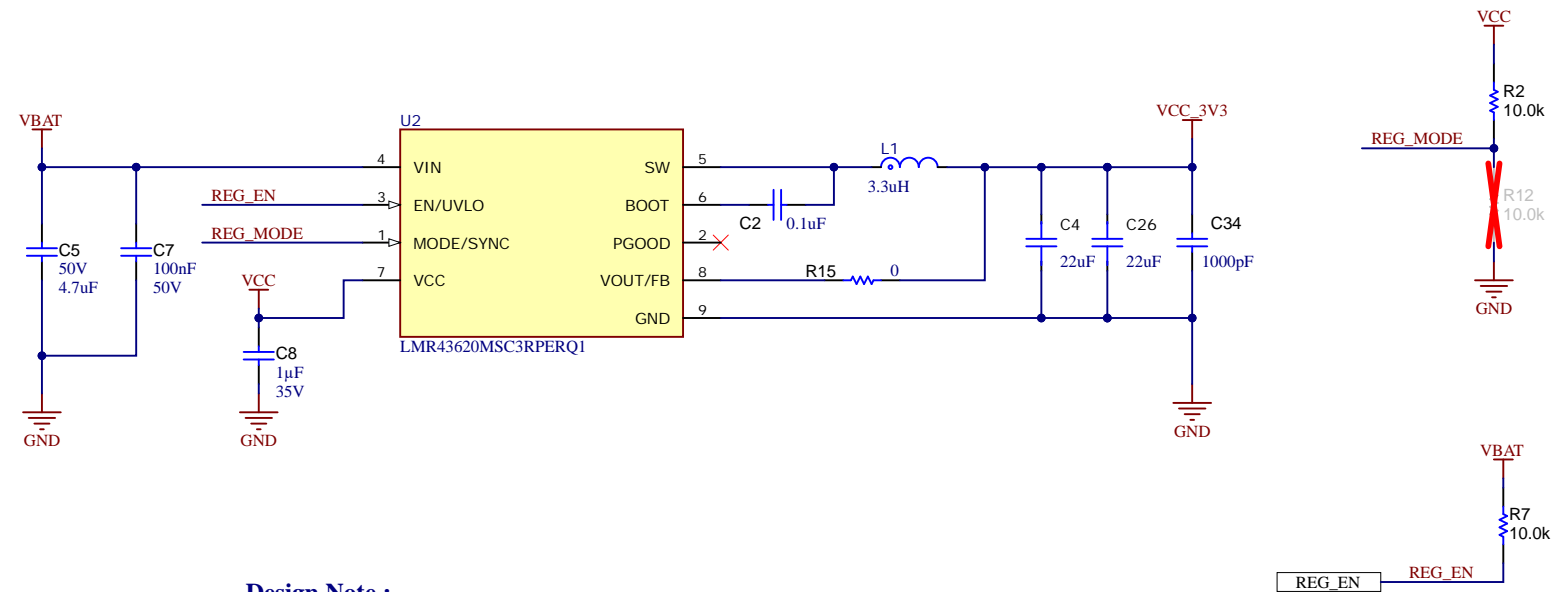
A

B

A

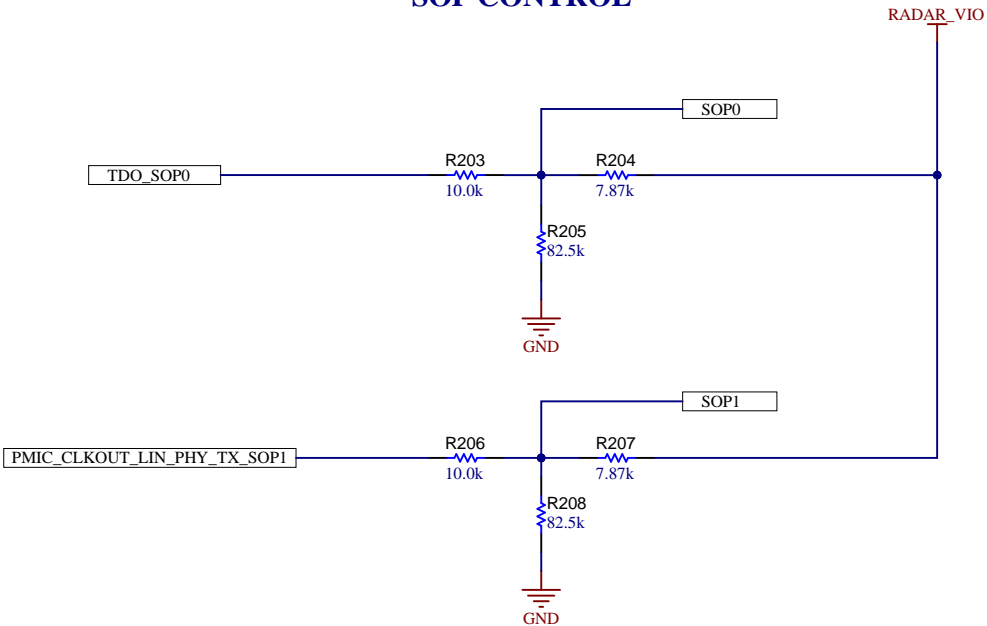
B

12V TO 3.3V BUCK CONVERTER



**Design Note :**  
Default set to FPWM mode, for setting to AUTO mode, mount R12 and DNP R2

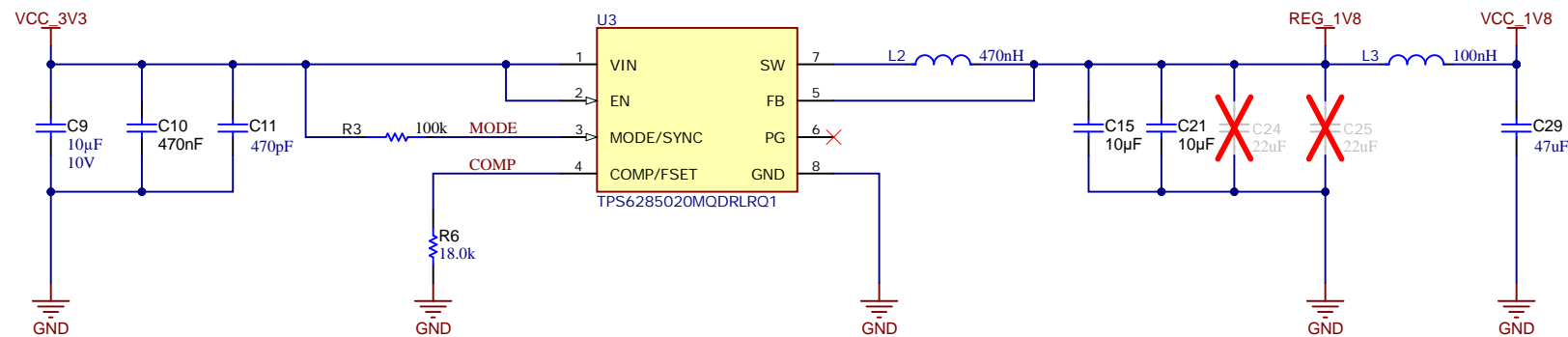
SOP CONTROL



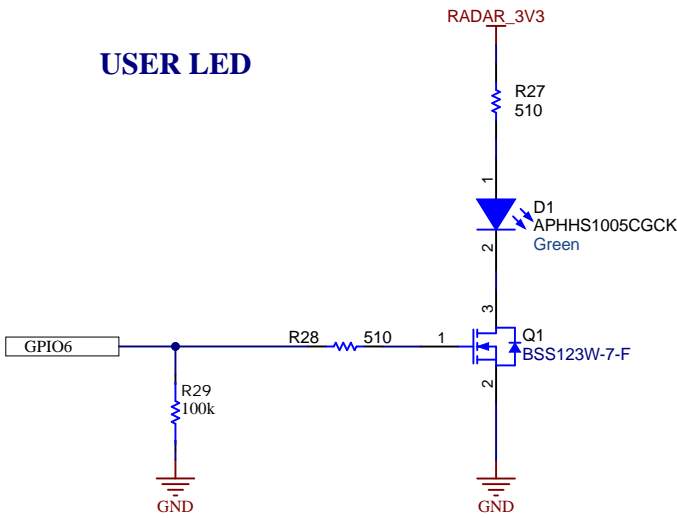
SOP CONFIGURATION

SOP Mode	PMIC_CLK_OUT, TDO	Combination
SOP_MODE1	Device Management Mode / QSPI flashing mode	0 0
SOP_MODE2	Application Mode / Functional Mode	0 1
SOP_MODE4	Debug Mode / mmWave Studio connectivity mode	1 1

3.3V TO 1.8V BUCK CONVERTER



USER LED



C

D

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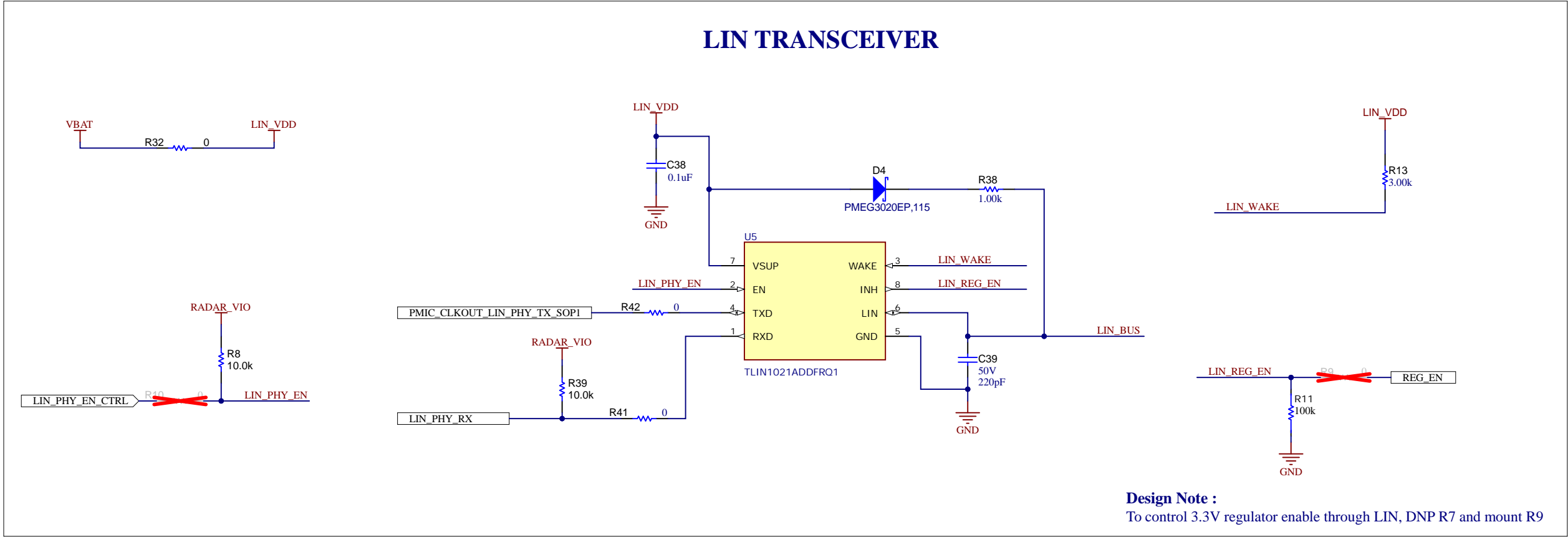
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Number: TIDEP-01036   Rev: A	Sheet Title: BUCK REGULATORS SOP CTRL	
SVN Rev: Not in version control	Assembly Variant: 001_AWR	Sheet: 5 of 7
Drawn By: Texas Instruments	File: AWRL1432KTO_Buck_Regulators_SOP_Ctrl.SchDoc	
Engineer: Texas Instruments	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

A

B

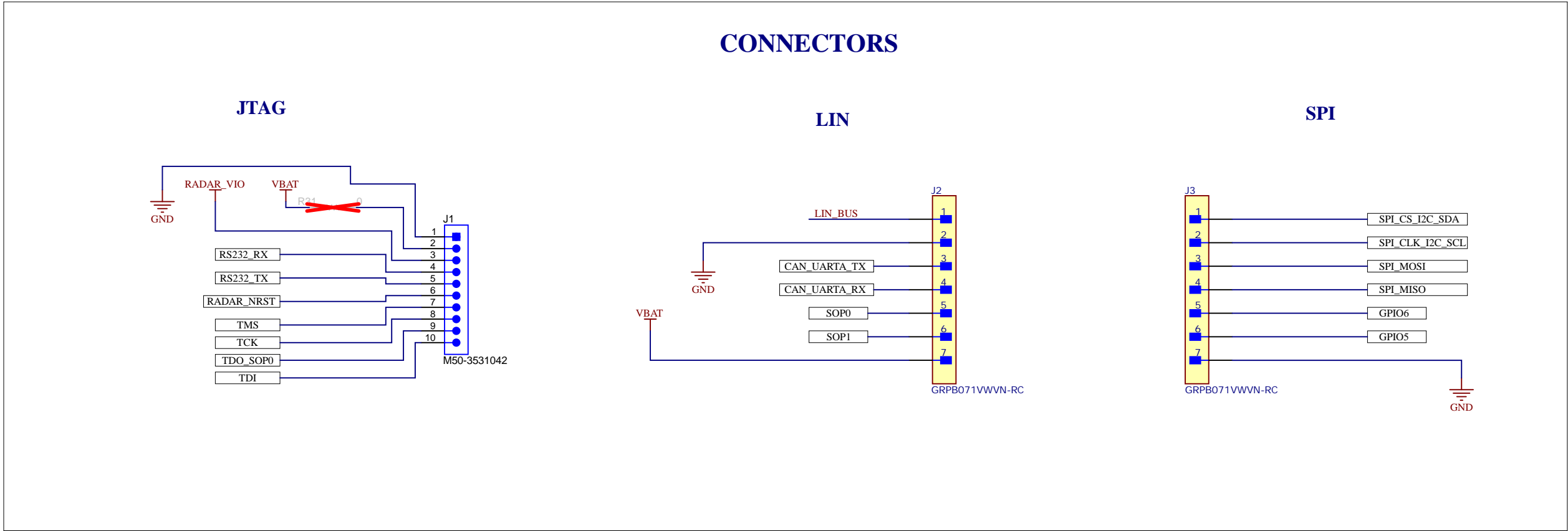
A

B



C

C



D

D



PCB Number: TIDEP-01036  
PCB Rev: A

PCB  
LOGO  
Texas Instruments



PCB  
LOGO  
FCC disclaimer

PCB  
LOGO  
WEEE logo

CAUTION HOT SURFACE1



CAUTION HOT SURFACE

Variant/Label Table	
Variant	Label Text
001_AWR	AWRL1432KTO

LBL1  
PCB Label

THT-14-423-10  
Size: 0.65" x 0.20 "

ZZ1  
Label Assembly Note  
This Assembly Note is for PCB labels only

ZZ2  
Assembly Note  
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3  
Assembly Note  
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4  
Assembly Note  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5  
Assembly Note  
INDICATION FOR COMPONENTS D\* ARE GIVEN AT THEIR CATHODE SIDE.

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